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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,974	01/15/2004	Jenoe Tihanyi	1890-0033	4260
7590 02/17/2005				
Maginot, Moore & Beck Bank One Tower 111 Monument Circle, Suite 3000 Indianapolis, IN 46204			EXAMINER	
			NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/757,974	Applicant(s) TIHANYI, JENOE	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12 and 13 is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☒ Claim(s) 1-11 and 14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01-15-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 8, 10 and 14 are objected to under 37 CFR 1.75(c) as being in improper form because multiple dependent claim 8 depends upon multiple claim 3; multiple claim 10 depends on multiple claim 3 and 8; multiple claim 10 depends on multiple claim 3 and 8. Claim 14 is an unacceptable multiple dependent claim wording because the claim does not refer back in the alternative only. Claim depends upon claims 12 and 12. See MPEP § 608.01(n). Accordingly, claims 8, 10, 11 and 14 are not been further treated on the merits.

The recitation “ the first resistor (R2)” in claims 5 and 6 does not have antecedent basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker (US Pat. 6,084,462) in view of Grover et al. (US Pat. 6,825,105).

Regarding claims 1 and 2, figure 2 of Barker shows a MOSFET circuit having reduced output voltage oscillations during a switch-off operation during which the current flowing through the circuit falls to zero, comprising:

a first MOS transistor (M2);

a second MOS transistor (M1); and the second MOS transistor (M1);

being provided with its source-drain path in parallel with the source-drain path of the first MOS transistor (M2) between a voltage source and reference-ground potential; and

a constant voltage element (zener diode D1) between gate of the first MOS transistor (M1) and gate of the second MOS transistor (M2). Note that the first transistor (M2) has a gate-source voltage (V_{gs2}) smaller than the gate-source voltage

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(Vgs1) of the second transistor (M1) thus the first transistor is larger than the second transistor (see US Pat. 6,285,246). Figure 2 of Barker does not show that the first and second MOS transistors comprises cells and the number of cells in the first transistor (M2) is greater than the number of cells in the second transistor. Figure 1 of Grover shows a transistor comprising a multiple of cells (Ct) for forming transistors having a reduction in source contact resistance (col. 5, lines 15-32). Therefore, it would have been obvious to those having ordinary skills in the art to replace the large first transistor (M2) with a transistor having a large number of cells taught by Grover and to replace the second transistor (M1) with a transistor having a smaller number of cells for forming transistors having a reduction in source contact resistance (col. 5, lines 15-32).

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foreign Application (JP 6-053 800) in view of Grover et al. (US Pat. 6,825,105).

Regarding claims 1-3, figure 3 of (JP 6-053 800) shows a MOSFET circuit having reduced output voltage oscillations during a switch-off operation during which the current flowing through the circuit falls to zero, comprising:

- a first MOS transistor (Q2);

- a second MOS transistor (Q4); and the second MOS transistor ; being provided with its source-drain path in parallel with the source-drain path of the first MOS transistor between a voltage source and reference-ground potential;

- a constant voltage element (zener diode SBD2) between gate of the first MOS transistor and gate of the second MOS transistor . Figure 3 (JP 6-053 800) does not show that the first and second MOS transistors comprises cells and the number of cells in the first transistor (M2) is greater than the number of cells in the second transistor; and

- a resistor (R2) coupled in parallel with the zener diode.

Figure 3 of (JP 6-053 800) does not show that the first and second MOS transistors comprises cells and the number of cells in the first transistor is greater than the number of cells in the second transistor. Figure 1 of Grover shows a transistor

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comprising a multiple of cells (Ct) for forming transistors having a reduction in source contact resistance (col. 5, lines 15-32). Therefore, it would have been obvious to those having ordinary skills in the art to replace the first transistor (Q2) with a transistor having a large number of cells taught by Grover and to replace the second transistor (Q4) with a transistor having a smaller number of cells for forming transistors having a reduction in source contact resistance (col. 5, lines 15-32).

Allowable Subject Matter

Claims 12 and 13 are allowed.

Claims 4-7 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12 and 13 are allowed because the prior art of record (US Pat. 6,084,462, US Pat. 6,825,105) fails to teach or suggest an integrated MOSFET circuit having reduced output voltage oscillations during a switch-off operation during which the current flowing through the circuit falls to zero comprising: a zener diode formed by a polycrystalline layer on a polycrystalline gate plane of the MOS transistors and a zone provided in the polycrystalline layer and having an opposite conduction type to the conduction type of the layer as called for in claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

02-09-04



MY-TRANG NUTON
PRIMARY EXAMINER

2/15/05